4G RF Systems On Chip or On Module?

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Abstract — **The present trend in the RF communications is to integrate as far as possible the function within a chip. Obviously the cost of a function mainly depends on the number of external components. The matter of this paper is to evaluate the limit of the integration looking at the economic topics and technical possibilities.**

I. Introduction

In this paper, around the limit of the integration for the next mobile generation, three examples will be presented in order to illustrate the discussion; a GSM/DCS receiver for the 2G mobile standards; a Bluetooth transceiver for the LAN approach and finally a multi-mode mobile receiver will cover the 3G mobile generation. A perspective beyond the 3G toward the 4G generations will be developed in conclusion.

II. The 2G Communication Standards [1]

In the 2G generation, standards based on GMSK modulation and TDMA access, with a narrow band channel, were developed. The table 1 summarizes main characteristics of such standard, while the table 2 gives an overview of the main RF Front End specifications

TABLE1
GSM & DCS Characteristics

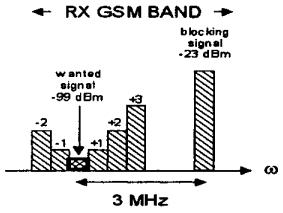
	GSM	DCS
Frequency RX	915 - 960 MHz	1805 - 1880 MHz
TX	880 - 915 MHz	1710 – 1785 MHz
Access Mode	TDMA/FDM	TDMA/FDM
Duplexing	FDD	FDD
Modulation	0.3 GMSK	0.3 GMSK
Coding	13 Kbit/s	13 Kbit/s
Data Rate	270.833 Kbit/s	270.833 Kbit/s
Channel BW	200 KHz	200KHz
Num. of Channels	124	1600

TABLE2
GSM & DCS RF Specifications

	GSM	DCS
IIP1	-13dBm	-13dBm
IIP3	-19dBm	-19dBm
NF	9dB	9dB
IR (Low IF)	> 35dB	> 35dB
PhiN@3MHz	-141dBc	-141dBc
Pout max	33dBm	30dBm

The main constraints of these standards are given below.

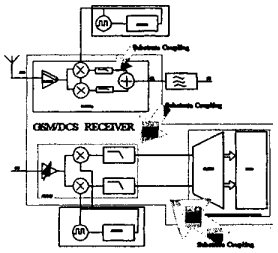
Figure 1
GSM & DCS Constraints



III. A 2G GSM/DCS Circuit

A GSM/DCS RF to Digital Monochip receiver is presented to illustrate the 2G integration. The purpose of this study was to evaluate the substrate coupling effects and to define a partitioning for 2G generation circuits. A synoptic of the circuit is given in the figure2.

Figure 2
GSM/DCS Receiver synoptic



In order to reach the Noise figure, the selectivity and the phase noise at a minimum power consumption, a 0.35um BiCMOS SiGe process with a 40GHz FT bipolar was selected. The partitioning as it is shown in the figure 2 is made by two main circuits, a RF- Analog Base Band one which includes the data converters and a FIR filter for the demodulation, (the presented circuit), in BiCMOS SiGe and a DSP for the Digital signal processing in VLSI CMOS. The transmission part was not implemented in this study, but should be implemented on the same RF-Analog circuit than the RX due to the fact that the standard is a TDMA one. The PPA could be implemented on the same chip too, due to the architecture selected, (super heterodyne), described in the figure 3.

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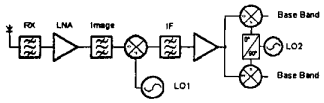
Figure 3
Super heterodyne architecture

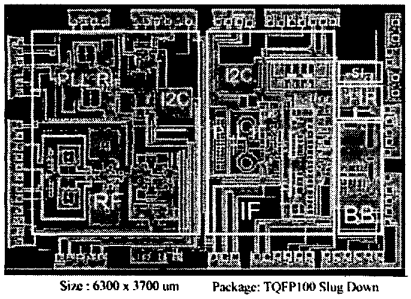


The advantages of this well known architecture are that the LO1 leakage on the antenna is negligible, there is no Image rejection thanks to the filter, and no DC offset. The targeted market being the mobile phone, the price of the final product must be as lower as possible. The selected package is a TQFP 100, which introduces a mandatory simulation of the coupling effects and losses due to the package and the substrate.
A presentation of the main measured results is given in the table3, followed by the micrograph of the circuit in the figure4.

TABLE 3
GSM-DCS Receiver measurements

Parameters	GSM	DCS
Power Cons	136mW	136mW
Low Gain	-6dB	-10dB
IIP1 LG	-14dBm	-14dBm
IIP3 LG	-7dBm	-7dBm
GMSK EVM	2.03% rms	2.25% rms
GMSK Mag Er	1.54% rms	1.48% rms
GMSK Phi Er	0.75°	0.97°
IQ offset	0.56%	1.87%
IQ Imbalance	0.55%	1.20%
Max Sensitivity	-107 dBm	-99 dBm
RF isolation	38.6 dB	40 dB
LO Leakage	-63.6 dB	-59.7 dB

Figure 4
GSM / DCS receiver Micrograph



Size : 6300 x 3700 um Package: TQFP100 Slug Down

The GSM/DCS results exhibit a good correlation between measurements and specifications that mean that a fully integrated RF to Digital Biband receiver in super heterodyne architecture is technically possible in SiGe BiCMOS process. The extra cost of external components, especially SAW filters, the extra cost of the process for the digital functions and the power consumption are the main drawbacks of this approach.IV. THE LAN COMMUNICATION STANDARDS [2]

In parallel, WLAN standards are under development. One of them, Bluetooth is mainly dedicated to the home access with an expected data rate less than 2Mbits. Main characteristics of this standard are summarized in the table 5, while the table 6 gives an overview of its main RF characteristics.

TABLE 5
Bluetooth characteristics

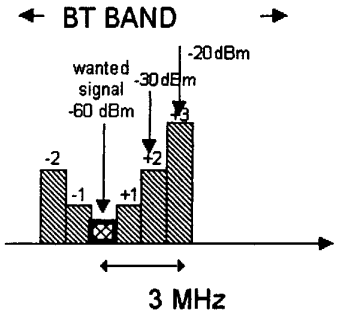
Frequency RX / TX	2400 – 2480 MHz
Access Mode	TDMA/FDM
Duplexing	TDD
Spectral spread	FHSS
Modulation	GFSK
Data Rate	640Kbit/s to 1Mbit/s
Channel BW	1MHz
Nb of Channel	79
Users/ channel	1

TABLE 6
RF specifications for Bluetooth

IIP1	-25dBm
IIP3	-16dBm
NF	20dB
IR (low IF)	>20dB
PhiN@2MHz	-121dBc
PLL Set-Time@75KHz	200us
Pout max 10m / 100m	0dBm / 23dBm

The figure5 explains the main constraints of this standard.

Figure5
Bluetooth constraints.

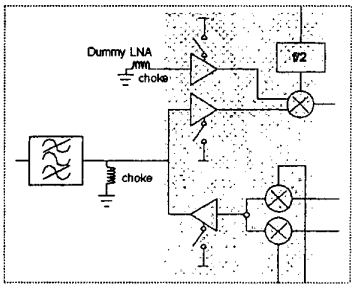


V. A W-LAN BLUETOOTH CIRCUIT

A Bluetooth Monochip transceiver is presented to illustrate the WLAN standard integration. This work faces

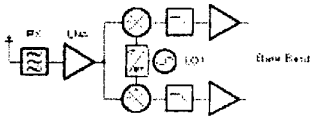
some of the ultimate challenging in order to achieve the fully integration, in particular the way to avoid the use of both external balun and antenna switch.
The figure 6 gives a synoptic of this circuit.

Figure6
Synoptic of the TX-RX Bluetooth Monochip



The partitioning of such function is simple, to reduce the cost of the application, the RF Front End and the Digital Base Band must be implemented in the same system on chip and the number of external components must be reduced as far as possible. The integration of such circuit was made in a 0.18um RF CMOS with a 50GHz FT.
The selected architecture, in order to reduce the die area and the consumption is a Zero IF one.

Figure7
Zero IF Architecture

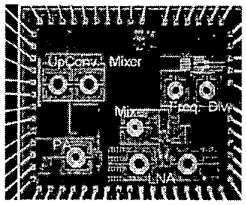


The advantages of such architecture are the high integration level, no image rejection requested, and low level of power consumption. The drawbacks are the sensitivity to DC offset and the flicker noise in the base band. The challenge of this design was to reduce the drawbacks and to evaluate the feasibility of this architecture for the Bluetooth standardFinally, the circuit was packaged in a TQFP 48, which introduces a mandatory simulation of the coupling effects and losses due to the package and the substrate.
A presentation of the main measured results is given in the table7, followed by the micrograph of the circuit in the figure9.

TABLE7
TX/RX Bluetooth Measurements

RX Mode	
Supply Voltage	1.8V
IIP3	>-10dBm
IIP1	>27dBm
P-1dB	>-16dBm
NF	16dB (ZIF), 10.8dB (LIF)
Gain	22dB
Mixer consumption	1.6mA
LNA consumption	1.4mA
RX to TX Isolation	>50dB
TX Mode	
Supply Voltage	1.8V
P-1dB	5dBm
Image Rejection	>22dB
Tuning Range	20dB
TX to RX Isolation	>50dB

Figure9
TX/RX Bluetooth photograph



The transceiver well matches the Bluetooth specifications independently from the receiver topology (LowIF, ZeroIF or Quasi ZeroIF). The chip does not need any external balun or an antenna switch. This approach demonstrates the possibility to integrate Bluetooth or such standard in the Base Band chip, or to go to a SOC approach.

VI. The 3G Communication Standards [3]

3G generation is based on the UMTS standards. Its main characteristics are given in the table8, and the main RFFE characteristics in the table 9.

TABLE8
UMTS WCDMA Characteristics

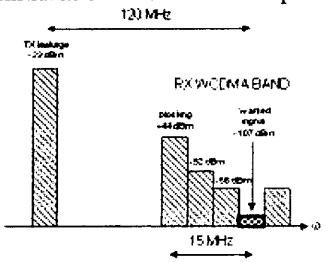
Frequency RX	2110 – 2170 MHz
TX	1920 - 1980 MHz
Access Mode	W-CDMA
Duplexing	FDD
Modulation	QPSK
Data rate	2048 Kbit/s
Filter	Cosine
Channel BW	5 MHz

TABLE9
WCDMA RFFE specifications

IIP1	-10dBm

IIP3	-1dBm
NF	9dB
IR (Low IF)	>51dB
PhiN@8MHz	-129dBc

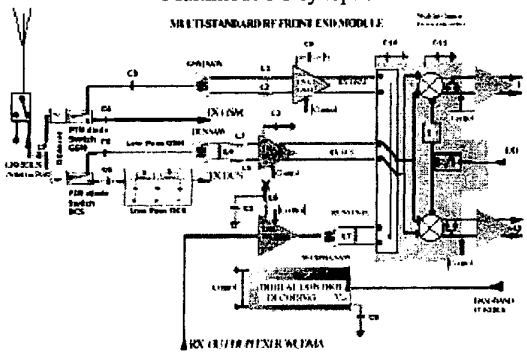
The main constraints of this standard are explained below.



VII. A MULTIMODE 3G EXAMPLE

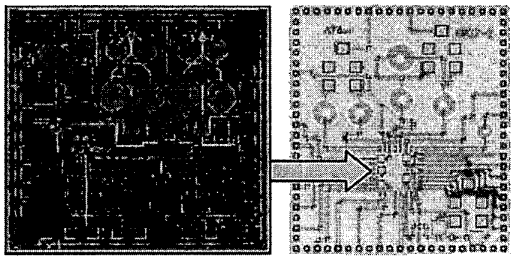
A W-CDMA GSM/DCS receiver is presented to illustrate the 3G standard integration. Due to the full duplex access in WCDMA, the Up link cant be implemented on the same chip than the Down link. The followed strategy for this design is a module approach for the RF Front End, in order to achieve a fully integration. The ASICS, Saw filters and PIN diodes are flip chipped on a Passive Devices Integrated glass module where the self inductors, capacitors and resistors are integrated. The figure 10 gives a synoptic of the mixed SiGe BiCMOS and PDI circuit.

Figure10
Multimode 3G synoptic



The selected architecture is Zero IF, the PDI allowing giving a very good isolation between the TX, RX paths and the synthesizer. The drawbacks of this approach are the extra cost of the PDI to be moderated by the cost of external components in a standard approach. This module is presently under evaluation with a good fit to the specifications. The main results will be presented in the conference. The figure 11 shows the two parts of the circuit, the ASIC on the left and the PDI on the right.

Figure 11
WCDMA GSM/DCS MultiMode ASIC and PDI



IV. IN CONCLUSION, THE 4G CIRCUITS

The partitioning of the functions depends on the constraints coming from the targeted standard, the silicon process availabilities, and cost efficiency of the selected architecture.

The future 4G circuits must integrate the present mobile standards up to 3G, one or two LAN standard, the GPS, and new modulation approach like Multi Carrier CDMA. That means that the RF Front End will need a specific DSP to manage its activity, the simplest standard like Bluetooth being integrated in this DSP. This is possible in a SiGe BiCMOS approach with a CMOS compatible to the leading edge VLSI integration level. In order to avoid the TX-RX and LO leakages, the PDI approach seems to be a good compromise. The Big Digital Signal Processor for Multi-mode Multi-access being integrated into a VLSI low cost CMOS process.

REFERENCES

[1] D.Belot,& all. *"A DCS 1800/ GSM 900 RF toDigital Fully integrated Receiver in SiGe 0.35um BiCMOS"* IEEE BCTM 01.

[2] B. Tait, *"The Ultimate Bluetooth Solution - Zero Chip less than 1$"*, Bluetooth conference, Edinburgh, October 2000.

[3] V.Aparin, & all. " *A highly-integrated Tri-Band/Quad Mode SiGe BiCMOS RF to BB Receiver for Wless CDMA:WCDMA/AMPS Application with GPS capability"* IEEE ISSCC 02.